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Dues. Change
Emails - Logan
2/25/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/652,550
Filing Date August 31, 2000
Inventor Keiji Jono et al.
Assignee KMT Semiconductor, LTD and Micron Technology, Inc.
Group Art Unit 2811
Examiner Q.D. Vu
Attorney's Docket No. KM1-001
TITLE: Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming
an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation
Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed
in a Semiconductor, Memory Cells and DRAMS

Assistant Commissioner for Patents
Washington, D. C. 20231
Attention: Official Draftsman


SUBSTITUTE DRAWING REQUEST

Enclosed is a Red-line drawing of Fig. 3 along with corrected formal drawings, Figs.
1-6. Please enter the enclosed substitute formal drawings in the above-referenced
application in place of drawings originally filed.

Acknowledgment of receipt of the formal drawings and their acceptance into the file
is requested.

Respectfully submitted,

Date: 2-6-03

By: 
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Enclosures: 1 Red-line Drawing Sheet, Fig. 3 & 3 Sheets of Formal
Drawings, Figs. 1-6.